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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations May-2022

SWITCHING THEORY AND LOGIC DESIGN

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

- 1 a State and Prove Demorgan's Theorem using suitable example. L3 6M
 b Simplify the following to a sum of 3 terms: L4 6M
 $A'C'D' + AC' + BCD + A'CD' + A'BC + AB'C'$
- OR**
- 2 a Express the following functions in sum of Minterms and product of Maxterms L2 6M
 i. $F(A,B,C,D) = B'D + A'D + BD$ ii. $F(x,y,z) = (xy + z)(xz+y)$
 b Express the following Boolean functions in to Canonical form: L2 6M
 i. $F=AB+BC+CA$ ii. $F= XY+Z+YZ+XYZ$

UNIT-II

- 3 Apply the K-Map technique to simplify the Boolean expression in POS and SOP form using K-map. Given: $F(A,B,C,D) = \Sigma(1,2,4,5,9,12,13,14)$ L4 12M
- OR**
- 4 a Deduce the following Boolean expressions using K-map and implement them using NAND and NOR gates: L4 6M
 (i) $F(W, X, Y, Z) = W'X'YZ' + W'XYZ' + WX'YZ' + WX'YZ + WXYZ' + WXYZ$
 b Explain the structure of Ex-OR gate by K-Map using 4 Variable. L2 6M

UNIT-III

- 5 a Define Combinational Circuit; explain the analysis procedure of a combinational logic circuit using suitable example. L2 6M
 b Design & implement Full Adder with truth table. L3 6M
- OR**
- 6 a What is multiplexer? Construct 4:1 multiplexer with logic gates and truth table. L3 6M
 b Design 32:1 Mux using two 16:1 MUXs and one 2:1 MUX. L3 6M

UNIT-IV

- 7 a Explain the working principle of D & T Flip-Flops. L2 6M
 b Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram. L2 6M
- OR**
- 8 a Design a 4 bit Decade counter. L4 6M
 b Explain in brief about a 3-bit synchronous up-counter. L4 6M

UNIT-V

- 9 a Distinguish between Melay & Moore machines. L2 6M
 b Explain the following related to sequential circuits with suitable examples L2 6M
 i) State diagram ii) State table
- OR**
- 10 Illustrate the PAL for the following Boolean function(i) L3 12M
 $F(A,B,C,D) = \Sigma m(2,3,8,9,10,12,13)$
 (ii) $G(A,B,C,D) = \Sigma m(1,3,4,6,9,12,14)$

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